REMARKS

Claim 1-19 are pending in the application. Reconsideration is respectfully requested.

In the outstanding Office Action, claims 2-9 and 11-18 were rejected under 35 U.S.C. 103(a) as being unpatentable over by U.S. Patent No. 6,469,354 (Hirata) in view of U.S. Patent No. 5,589,423 (White et al.); and claims 10 and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata in view of White et al. and further in view of Applicant's Admitted Prior Art (AAPA).

Rejections under 35 U.S.C. Section 103

Claims 2-9 and 11-18 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata in view of White et al. Applicants respectfully traverse the rejection.

Hirata discloses a semiconductor device that includes a protective circuit at an input/output port that further includes a plurality of protective MOS transistors.[1] In particular, Hirata discloses input/output circuit sections composed of paired nMOSFETs **31** and pMOSFETs **32**.[2] Further, Hirata discloses the drain regions **14n** of the nMOSFET **31** and the drain regions **14p** of the pMOSFET **32** are connected to another pad **22** via another interconnect **14a**.[3] Further, Hirata discloses the gate electrodes **15n** and **15p** are connected to an output of an un-illustrated output pre-buffer of the internal circuit.[4]

Further, Hirata discloses that the drain **14n** and the source **16n** are formed of an *N+ diffused layer*, and a portion of the P-well **11** located beneath the gate **15n** is of a P-conductivity type, *an NPN parasitic transistor* **12** is formed beneath the gate **15n**.[5] Further, Hirata discloses the drain **14n** corresponds to a collector **14c**, a P-well **11** corresponds to a base **11c**, and the source **16n** corresponds to an emitter **16c** of a parasitic transistor **12**.[6] Furthermore, Hirata discloses the collector **14c** is connected to a pad **22**, and the emitter **16c** is connected to the *ground* together with the guard ring **18n**.[7] Moreover, Hirata discloses a

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[1] Hirata at ABSTRACT.
[2] *Id.* at column 2, lines 4 -5.
[3] *Id.* at column 2, lines 5 - 6.
[4] *Id.* at column 2, lines 6 - 8.
[5] *Id.* at column 2, lines 53 - 56.
[6] *Id.* at column 2, lines 57 - 59.
[7] *Id.* at column 2, lines 60 - 62.

parasitic resistor **17** is formed between the base **11c** and the guard ring **18n**.[8]

However, Hirata nowhere discloses, as claims 2 and 11 clearly recite:

> *a silicide blocked p-type field effect transistor* having a source, drain, gate, and gate oxide, said transistor further *having a snapback voltage that is less than the breakdown voltage* of said gate oxide and
>
> wherein said gate is positioned between a p-diffusion of said source and a p-diffusion of said drain,
>
> an n-diffusion is directly connected to said gate and said p-diffusion of said source and the n-diffusion is spaced apart from said p-diffusion of said source,
>
> said transistor is coupled to an I/O pad that is connected to said p-diffusion of said drain, and
>
> the I/O pad has no connection to n-diffusions of said transistor.

That is FIG. 3A of Hirata discloses *an n-type MOSFET* **31** configuration as opposed to "a silicide blocked *p-type field effect transistor,*" as recited in claims 2 and 11. Further, since the structure of Hirata is *not* identical to the claimed device as suggested in the outstanding Office Action, Hirata nowhere discloses, as recited in claims 2 and 11, "said transistor further *having a snapback voltage that is less than the breakdown voltage* of said gate oxide" (emphasis added).

Further, in contrast to FIG. 3A of Hirata, FIG. 7 of the specification clearly shows and claims 2 and 11 recite, "said gate is positioned between a *p-diffusion* of said source and p-diffusion of said drain" (emphasis added). In contrast to the recitations of claims 2 and 11 and the illustration of FIG. 7 of the specification, Hirata clearly discloses, as shown in FIG. 3A, a gate **15n** is positioned between *a N+ diffused area* **16n** of the source and an *N+ diffused area* of the drain **14n**.

Furthermore, in contrast to FIG. 3A of Hirata, FIG. 7 of the specification clearly shows and claims 2 and 11 recite, "an *n-diffusion* is directly connected to said gate and said *p-diffusion* of said source" (emphasis added). In contrast to the recitations of claims 2 and 11 and the illustration of FIG. 7 of the specification, Hirata clearly discloses, as shown in FIG. 3A, a *P+ type* guard ring **18n** is directly connected to said gate **15n** and an *N+ diffused area* **16n** of said source.

[8] *Id.* at column 2, lines 62 - 63.

Moreover, even if the alternative p-type MOSFET 32 is considered, Hirata nowhere discloses, as recited in claims 2 and 11:

> said transistor is *coupled to an I/O pad* that is connected to said p-diffusion of said drain, and
> the *I/O pad* has no connection to n-diffusions of said transistor (emphasis added).

That is, Hirata nowhere discloses the "I/O pad," recited in claims 2 and 11 and shown in FIG. 7 as reference 705. Thus, the structure of Hirata is *not* identical to the claimed device as suggested in the outstanding Office Action. Therefore, it is respectfully submitted that Hirata nowhere discloses, suggest or makes obvious the invention of claims 2 and 11.

In addition, the outstanding Office Action acknowledges other deficiencies in Hirata and attempts to overcome these deficiencies with White et al.[9] However, White et al. cannot overcome the deficiencies of Hirata as discussed below.

White et al. discloses a process for fabricating a non-silicided region in an integrated circuit.[10] However, White et al. nowhere discloses, as claims 2 and 11 recite:

> said transistor is *coupled to an I/O pad* that is connected to said p-diffusion of said drain, and
> the *I/O pad* has no connection to n-diffusions of said transistor (emphasis added).

That is, White et al. cannot overcome the deficiencies of Hirata, as discussed above.

Therefore, it is respectfully submitted that neither Hirata nor White et al. disclose, suggest or make obvious the claimed invention, whether taken individually or in combination, and therefore, claim 2 and claim 11, and claims dependent thereon, patentably distinguish thereover.

Claims 10 and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata in view of White et al. and further in view of AAPA. Applicants respectfully traverse the rejection.

Claims 10 and 19 are ultimately dependent upon claims 2 and 11, respectively. Thus, at least for the reasons discussed above, neither Hirata nor White et al. disclose, suggest or make obvious the invention of claims 10 and 19.

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[9] Outstanding Office Action at page 3, lines 17-19.
[10] White et al. at ABSTRACT.

In addition, the outstanding Office Action acknowledges deficiencies in Hirata and White et al. and attempts to overcome these deficiencies with AAPA.[11] However, AAPA cannot overcome the deficiencies of Hirata and White et al. as discussed below.

The AAPA discloses a circuit configuration of the background art typical of a latch-up condition.[12] However, it is respectfully submitted that the circuit configuration of the AAPA is not analogous to the recitations in claims 2, 10, 11 and 19. In particular, claims 2 and 11 recite:

> said transistor is *coupled to an I/O pad* that is connected to said p-diffusion of said drain, and
> the *I/O pad* has no connection to n-diffusions of said transistor (emphasis added).

Moreover, claim 10 recites: a "p-type resistor is located between a p-diffusion of said drain of said transistor and said I/O pad" and claim 19 is similarly worded. That is, in the invention of claims 2 and 11, the I/O pad is connected to a *p-diffusion drain* of the transistor. Thus, in claims 10 and 19, the "p-type resistor" is located between the I/O pad and "a p-diffusion drain" of said transistor."

In contrast to the claimed invention, the AAPA discloses a resistor **R** located between an **INPUT PAD** and diodes **D1, D2**. That is, the AAPA nowhere discloses resistor R as connected to a "p-diffusion drain," as clearly recited in claims 10 and 19. Thus, it is respectfully submitted that, the AAPA does not disclose the limitations of claims 10 and 19 and cannot overcome the deficiencies of Hirata and White et al.

Therefore, it is respectfully submitted that none of Hirata, White et al. and AAPA, whether taken individually or in combination, disclose, suggest or make obvious the claimed invention and that claims 10 and 19, and claims dependent thereon, patentably distinguish thereover.

[11] Outstanding Office Action at page 5, lines 15-17.
[12] Specification at page 3, lines 20-25.

Conclusion

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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